A Constant Fraction Discriminator with Shape-Agnostic Fraction Triggering and Sub-ns Walk for the Solar Probe Analyzer for Ions

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***Abstract*—Electrostatic analyzers like the Solar Probe Analyzer for Ions can use time-of-flight techniques to determine the ion composition of space plasmas. The conversion of trigger events to their digital equivalent is a central component of any timing-based front end, with integrated solutions increasingly desirable for constrained size, weight, and power budgets. Conventional analog methods of pulse discrimination introduce timing walk or are limited to a narrow set of pulse shapes, while digital methods require impractically high sample rates for the allowable power consumption. This work presents an integrated constant fraction discriminator with theoretically zero timing walk and a well-defined and programmable trigger fraction that does not depend on input pulse shape. The test chip was fabricated in 0.18 µm bulk CMOS with 3 mA of current drawn from an internally regulated 1.8 V supply, and a measured timing walk of 601 ps over a 10x change in input pulse amplitude with a worst case jitter of 743 ps.**

***Index Terms*—constant fraction discriminator, time walk, time of flight, single event upset, watchdog, integrated circuit**

I. Introduction

The Solar Probe Analyzer for Ions (SPAN-Ion) is an electrostatic analyzer that uses a time-of-flight mass spectrometer to measure the ion composition of solar wind plasma, distinguishing ions' mass/charge ratios by measuring the time they take to traverse a 2 cm gap after acceleration with a -15 keV potential [1]. The endpoints of the gap are marked with carbon foils which produce secondary electrons upon impact with the incoming ion; those secondary electrons are then directed to a microchannel plate (MCP) particle detector which acts as an electron amplifier to produce current pulses approximated as Eq. (1)

$$I(t) = \frac{Q}{\tau_f - \tau_r}\left(e^{-t/\tau_f} - e^{-t/\tau_r}\right) \tag{1}$$

where Q is charge, and $\tau_r < 1\text{ns}$ and $\tau_f \approx 1\text{ns}$ can be thought of as rising and falling time constants. Variations in MCP gain and carbon foil yield produce current pulses which vary by up to an order of magnitude in amplitude. Previous versions of ion mass spectrometers have used a combination of discrete components and application-specific integrated circuits (ASICs) for pulse discrimination with a Z-stack MCP. However, tightening constraints on size, weight, and power have driven a shift toward integrated pulse discrimination, and demands for increased instrument throughput have replaced the Z-stack MCP with a chevron MCP with significantly reduced gain.

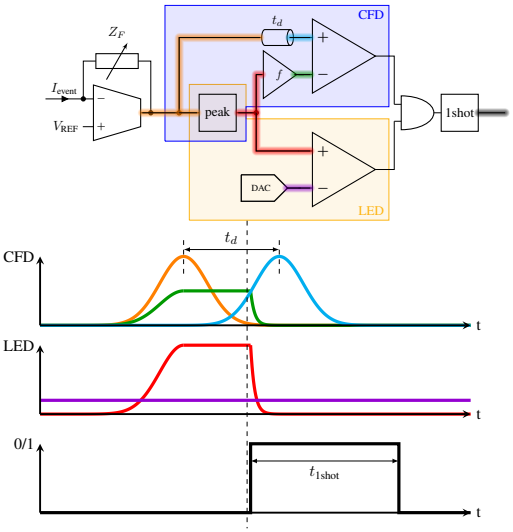


Fig. 1: Block diagram of the front end and its operation, with the CFD branch outlined in blue and the LED branch outlined in gold. The one shot output is used to reset the peak detector.

High precision pulse discrimination of analog signals is a well-studied problem with a wide variety of techniques [2]–[7] and implementations with varying levels of integration. In this work, we analyze prior methods in the context of SPAN-I and present a fully integrated pulse discriminator with zero theoretical dependence on pulse amplitude, a well-defined trigger fraction, and a measured timing walk of 601 ps over a 10× change in pulse amplitude. As a matter of practicality, the device incorporates afterpulse rejection, maintains a monotonic output vs. event rate, and is immune to single event upsets (SEU).

II. Design and Methods

A. Pulse Discrimination

Immediate digitization of the input signal allows for signal processing that scales well with process technology [8], [9]. Unfortunately, driving one minimum size transistor in a clock in 180 nm CMOS from a 1.8 V supply consumes more than $100\,\frac{\mathrm{nW}}{\mathrm{GHz}}$. An ADC with the requisite sampling rate and resolution would be impractically power-hungry and complicated by nominal transistor $f_{\max}$ and f_T in the tens of gigahertz. We opted for an analog constant fraction discriminator with shape-agnostic fractional triggering for our pulse timing discrimination.

Leading edge discrimination and constant fraction discrimination [10]–[12] are popular and well-established methods of pulse discrimination. Leading edge discriminators (LEDs) are the simplest method where the input is compared against a fixed threshold. However, this introduces timing walk where the output trigger's timing shifts with the input pulse's amplitude, making LEDs unsuitable for precision applications. While LED walk compensation techniques [2]–[4] are performed in the digital domain and so scale well, they require significant application- and sensor-specific calibrations

By contrast, constant fraction discriminators (CFDs) trigger relative to a constant fraction of the input pulse's peak, resulting in an output trigger with theoretically zero timing walk. The core of CFDs often generalizes in the time domain as Eq. (2)

$$s_{\text{out}}(t) = \operatorname{sgn}[s_{\text{in}}(t) * (h_+(t) - h_-(t))] \tag{2}$$

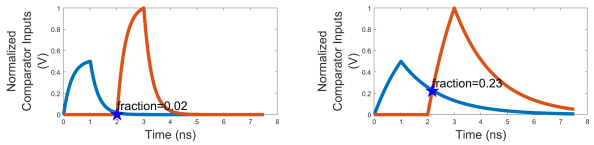
where $h_+(t)$ and $h_-(t)$ are the impulse responses of linear time-invariant operations $H_+(s)$ and $H_-(s)$; the signum function is a comparator. As long as the input signal s_{in} is scaled by a nonnegative value, the output s_{out} will remain unchanged. The specifics of H_+ and H_- vary, though a common variant uses a delay for H_+ and an attenuator for H_- [1], [6]. The attenuator enables tuning for the trigger fraction, and the delay ensures H_+ and H_- remain linear by avoiding signal clipping [5], [7]. However, this results in a circuit whose trigger fraction changes with pulse shape, which once again requires substantial calibration or else limits its utility across the breadth of pulse shapes.

B. Front End Architecture

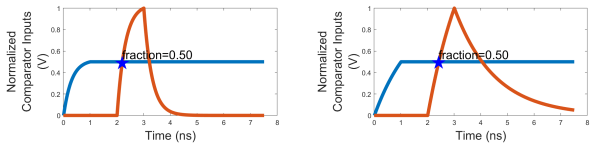
Fig. 1 shows the circuit and operation of the CFD architecture. A programmable transimpedance preamplifier converts the incoming charge or current pulse into a low pass filtered voltage while reducing the bandwidth and power requirements of downstream circuitry. An LED branch distinguishes the pulse from noise while the CFD branch provides the timing for pulse discrimination. A non-retriggering one-shot pulse generator maintains a monotonic relationship between event and output count rate, fixes the duration of the digital output pulse for off-chip circuitry, and rejects MCP afterpulsing.

For the CFD, we modified the delay-versus-attenuate architecture [1], [6], [13] by inserting a peak detector to track the maximum of the pulse over time. When used with a delay t_d greater than the time it takes the initial pulse to go from $f\times$ its peak to its peak, this guarantees that the CFD will always trigger at the fixed constant fraction f of the initial pulse's maximum, with an additional fixed offset of t_d from the delay (Fig. 2).

Another advantage over prior CFD architectures is the relaxation on the upper bound of t_d, even with extremely simple arming logic. In conventional delay-versus attenuate front ends, using only a simple AND gate at the CFD and LED outputs requires t_d be no longer than the duration of the input pulse. Rather than introduce additional hardware, we take advantage of the peak detector's memory and are able to extend the upper bound on the delay t_d by the minimum time between input pulses. For a sensor element which produces pulses $\approx$1 ns wide at an absolute maximum rate of of 10^7 pulses per second [1], this corresponds to an increase in the allowable range of t_d by one to two orders of magnitude, subject to leakage from reset switches and the storage capacitor in the peak detector.



(a) Conventional CFD



(b) Modified CFD

Fig. 2: Example inputs to the CFD comparator, (b) with and (a) without the peak detector inserted in the shaping chain. Orange is the delayed input, blue is the input attenuated by $f = 0.5$.

Because the peak detector has memory, single event transients (SETs) from ionizing radiation can cause the peak detector to hold radiation-induced pulses which do not correspond to pulses on the peak detector's input. Sufficiently large transients can make the LED trigger without the CFD and lock the CFD comparator low, effectively disabling the front end. To prevent system lockout, we introduce a watchdog (Fig. 3) to identify pulses on the output of the peak detector which do not correspond to its input. The watchdog determines if an LED rising edge has no associated CFD counterpart by waiting out a one shot generated timing pulse for t_{stuck} time, then asserting a reset on the peak detector if a corresponding CFD edge does not occur.

C. Block Implementations

All voltage DACs used outside of power management are identical 512-element resistive ladder tapped out by an 8-bit

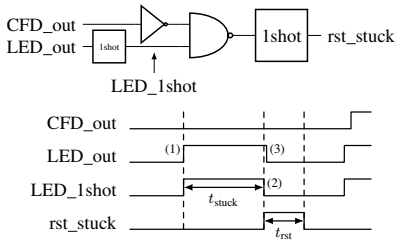


Fig. 3: The SET detection/correction watchdog circuit and operation in the event of an otherwise lock-inducing transient. (1) An SEE causes the peak detector output to trigger the LED, starting the LED_1shot timer. (2) If the CFD has not registered an event after t_{stuck}, rst_stuck raises, (3) resetting the peak detector along with the LED (and CFD) outputs.

binary mux at 256 contiguous sections. The selection of only half of the elements of the resistive ladder was to reduce the size of the mux, since the upper range of the 512-element ladder is not necessary for signal chain performance. The asynchronous nature of events and power constraints makes high speed clocked comparators impractical, so all comparators are cascades of five identical open loop amplifiers, biased for low gain and high bandwidth. All stages are fully differential, with differential nodes placed as close together as possible to increase the likelihood of radiation events appearing only in the common mode. The peak detector is a classic diode architecture with an output buffer and multiple feedback, with the reset tied to the logic OR of the final output pulse, the chip configure toggle, and an error correction signal from the SEE watchdog (Fig. 3). The resistive passive attenuator includes a reference node for DC cancellation given $V_{\text{REF}} \neq 0\text{V}$ for the preamplifier. The on-chip delay was implemented as a second order low pass Bessel filter, implemented in the Sallen-Key topology.

All digital cells are triple redundant with three majority voters between each logic gate stage for SEU immunity. Mutually redundant nodes are spaced in layout to minimize the risk that a single radiation event can affect more than one of the three copies and propagate the error to the next logic stage. Digital latches use dual interlocked storage cells (DICE) [14] in lieu of conventional latch topologies. As a result, more than one of four nodes in a cell must be flipped simultaneously in order for the cell's overall output to latch to an incorrect value.

III. Experimental Setup and Results

The test front end was fabricated in 0.18 µm bulk CMOS on a 1.6×1.7 mm^2 die. Chip power was internally regulated from an external 3.3 V supply to a 1.8 V core voltage. All DC pads for power and DACs were provided 10 nF of external decoupling capacitance to reduce supply bounce and voltage noise. The preamplifier bias V_{REF} and the reference for the attenuator were set at mid-rail, and the on-chip delay was set to its maximum of roughly 12 ns—more than twice the preamplifier's time constant.

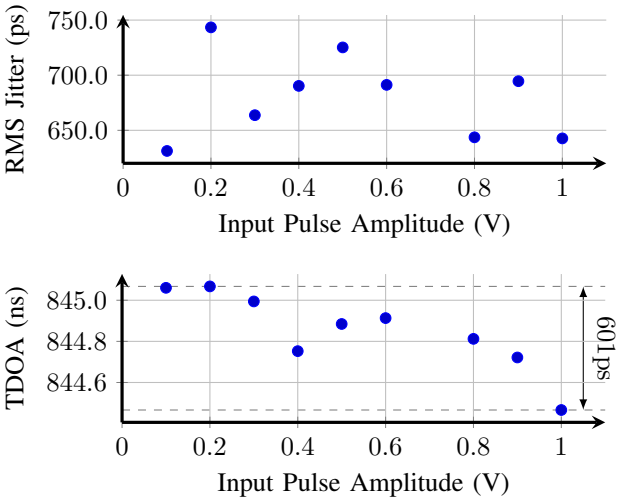


Fig. 4: TDOA and RMS jitter.

Timing walk and jitter were calculated from the time difference of arrival between a START pulse and the digital output (STOP) pulse of the front end, and was measured using a Texas Instruments TDC7200 time-to-digital converter.

A DG535 pulse generator with a 04B attachment for 100 ps falling edges produced negative voltage pulses nominally 2 ns wide with amplitudes ranging from 0.1 V to 1 V. The voltage pulses were connected with a 50 Ω termination to the PCB and AC coupled with a 2 pF capacitor for current pulses of 1.2 mA to 12 mA into the preamplifier. Each pulse amplitude test was repeated 500 times with at least 100 ns between pulses.

Fig. 4 shows time difference of arrival (TDOA) statistics between the START and STOP pulses after calibration to account for walk and jitter from the PCB and external components. After PCB calibration, the chip demonstrated a timing walk of 601 ps and a worst case RMS jitter of 743 ps across the range of input steps. Remnant walk is due to finite comparator bandwidth.

IV. Conclusions

We designed and tested a constant fraction discriminator for time-of-flight systems with sub-nanosecond timing walk and jitter, and whose modified architecture enables it to trigger on a constant fraction regardless of input pulse shape with internal delays longer than the input pulse's width. An output monostable multivibrator provides afterpulse rejection at the circuit level for a wide range of sensor elements. Triple voted gates and DICE latches ensure SEU immunity in digital hardware, while a similarly triple redundant watchdog prevents system lockout from SETs. Average current consumption was 3 mA from the on-chip 1.8 V regulator.

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