A Constant Fraction Discriminator with Shape-Agnostic Fraction Triggering and Sub-ns Walk for the Solar Probe Analyzer for Ions

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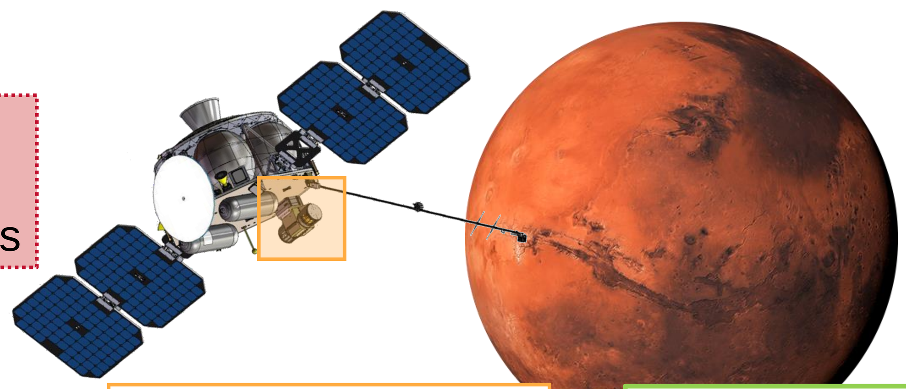
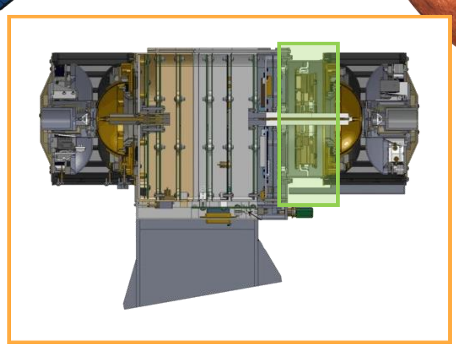
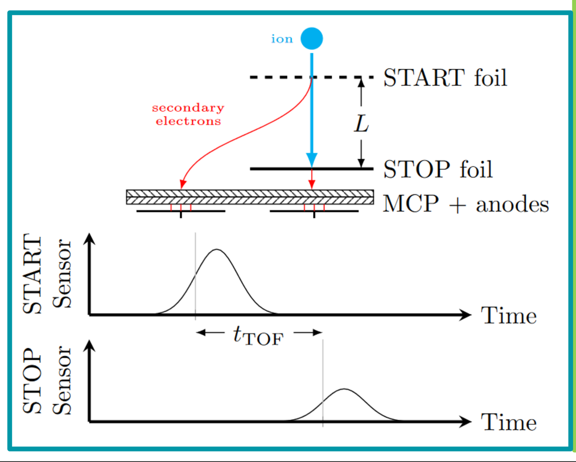
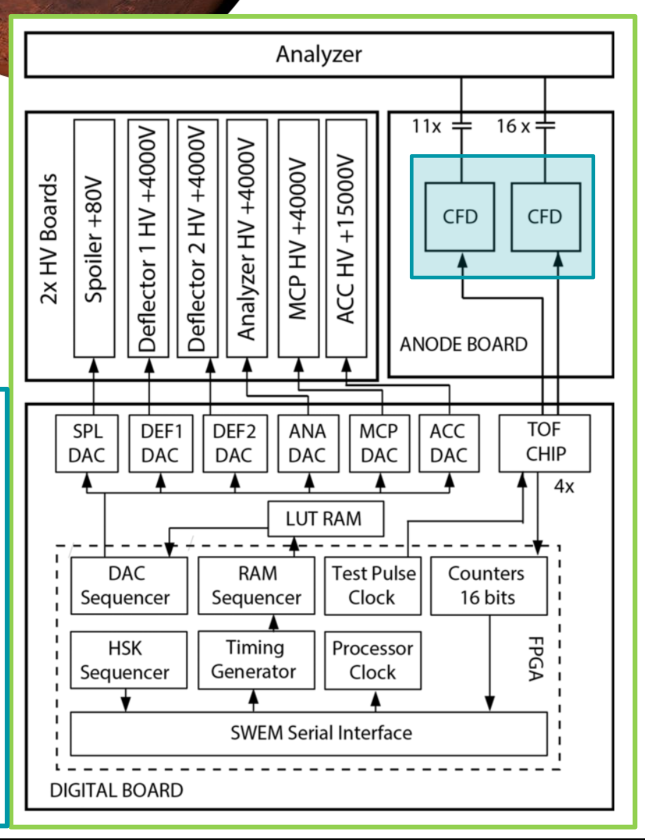
High Level: The Solar Probe Analyzer for Ions (SPAN-Ion)

1. Monitor and study the behavior of the solar wind + coronal plasmas
2. Measure the ion composition and distribution of the solar wind via time-of-flight mass spectrometry
3. Precisely mark the digital rising edge of variable-amplitude analog pulses



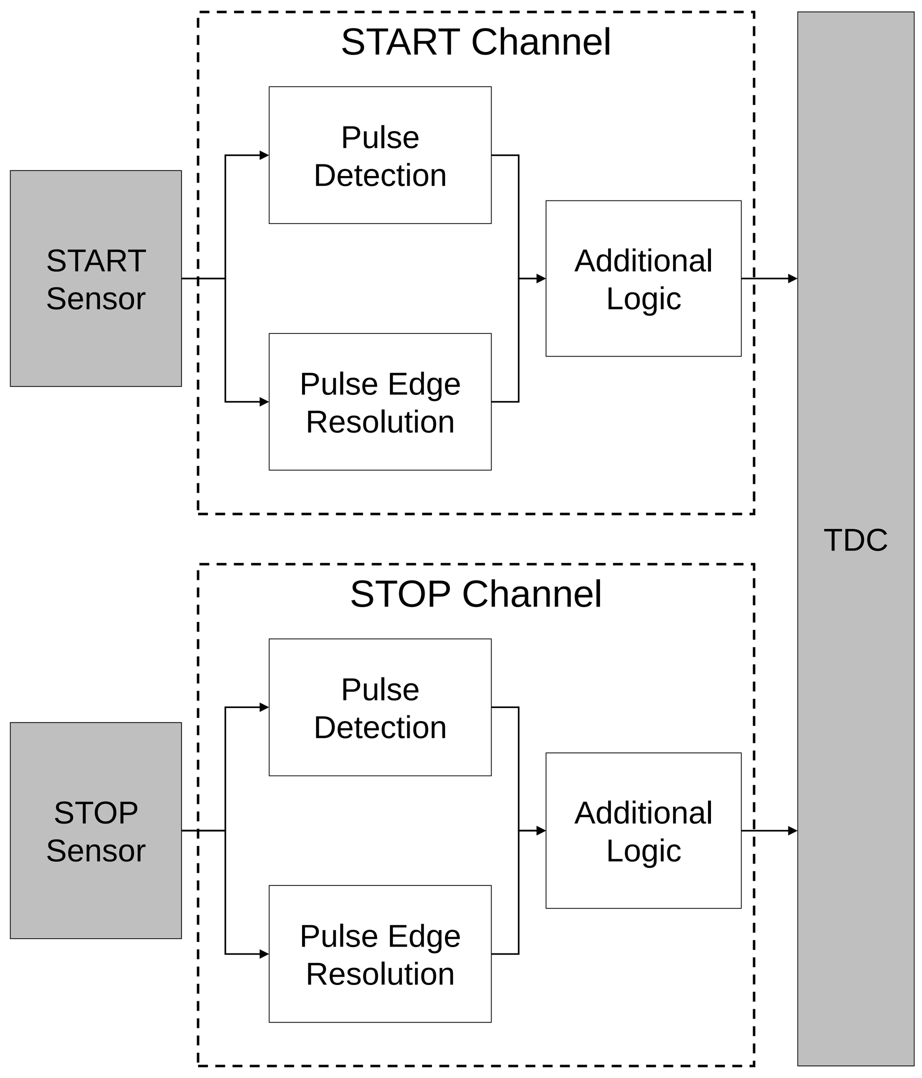






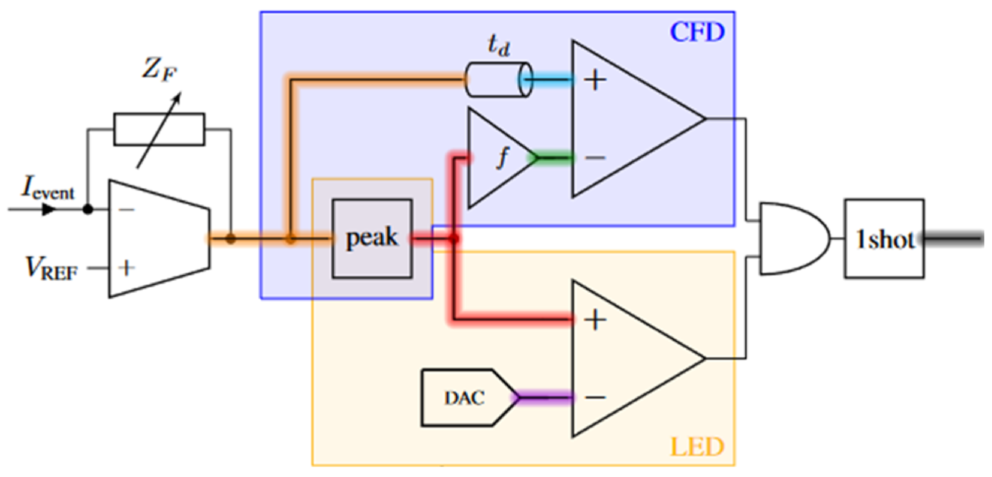
Frontend Objectives

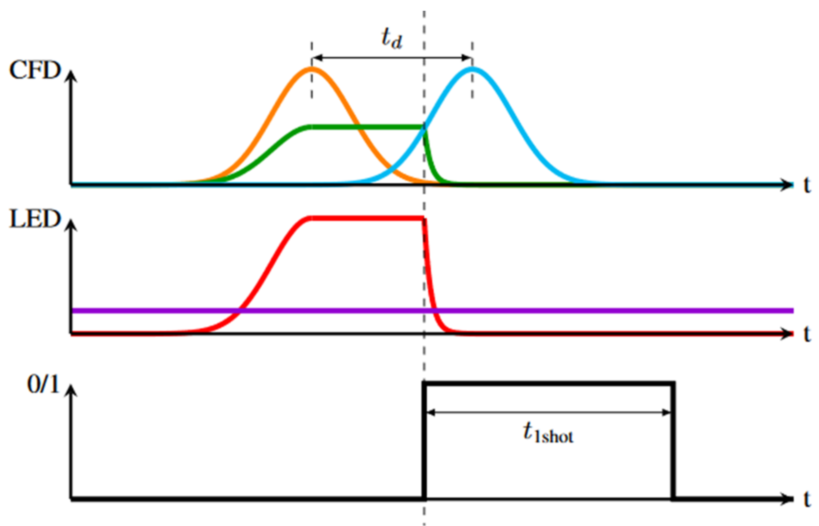
1. Pulse height-independent timing discrimination
2. <2 output triggers per event
3. Monotonically increasing count rate versus event rate
4. Tunable trigger point
5. No clipping
6. Radiation hardened by design (100krad, SEU immune)



Frontend Architecture

Constant Fraction Discrimination/Discriminator (CFD): The frontend triggers relative to a constant fraction of the input's peak. This produces an output edge whose timing is independent of the pulse's amplitude (zero timing walk).

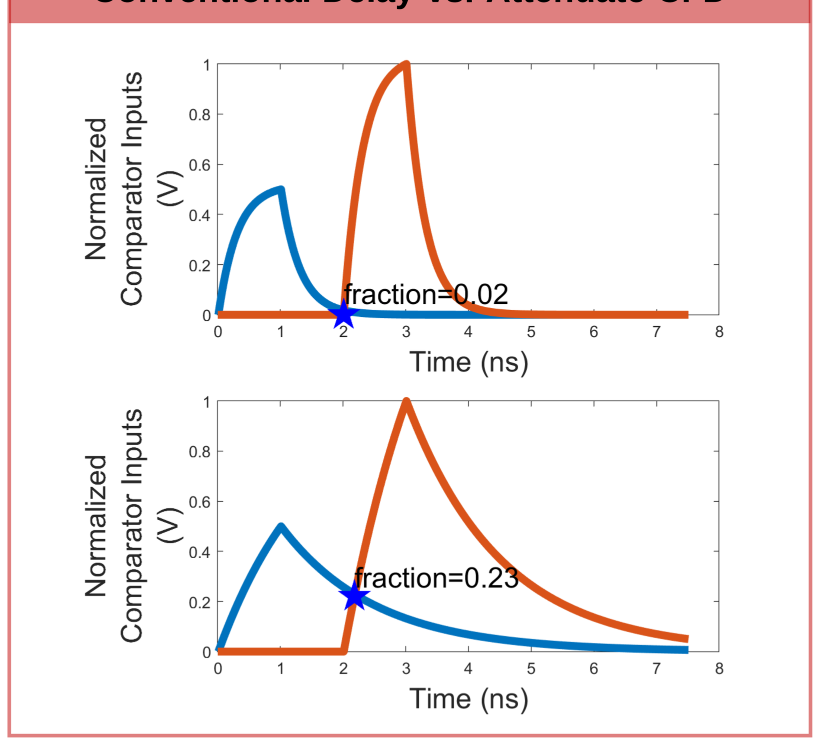




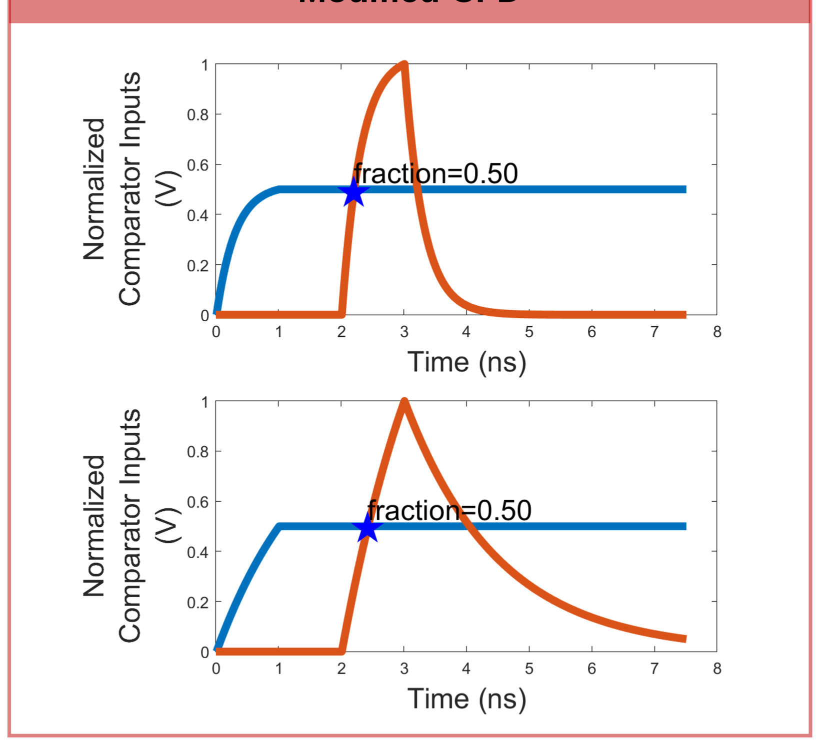
Additional peak detector in delay-versus-attenuate CFD:

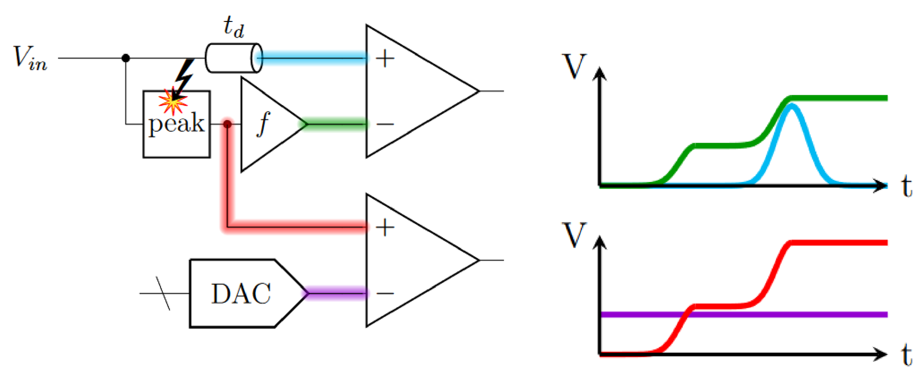
- Guarantees a constant trigger fraction f, regardless of pulse shape.
- Upper bound on t_d extends from pulse duration (~1ns) to time between pulses (>100ns).

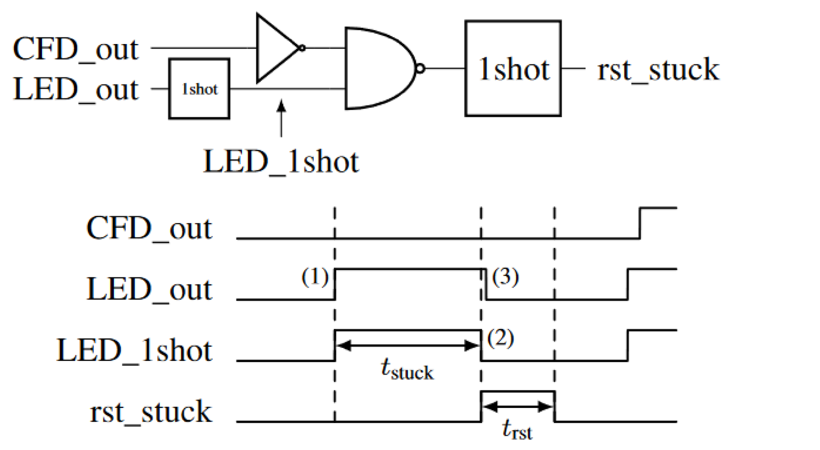
Conventional Delay-vs.-Attenuate CFD



Modified CFD

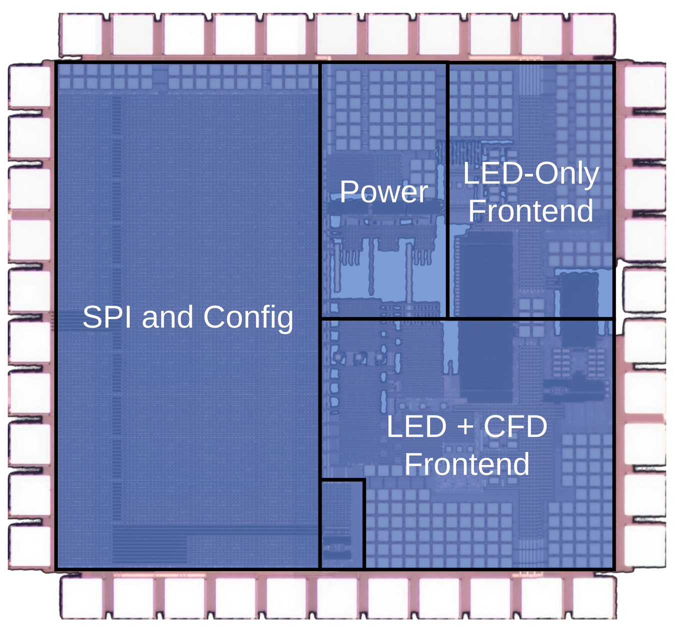




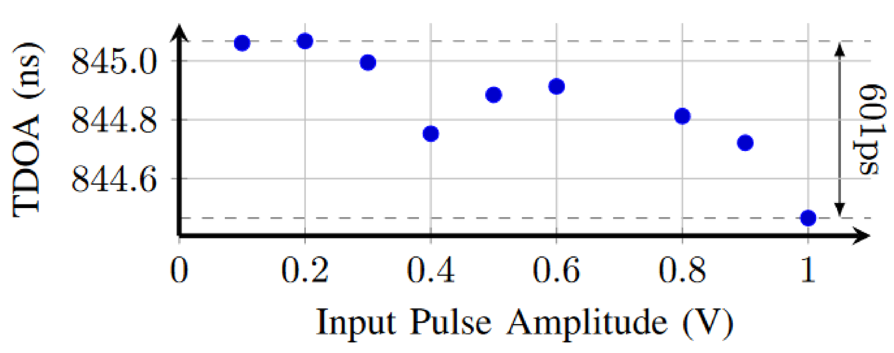


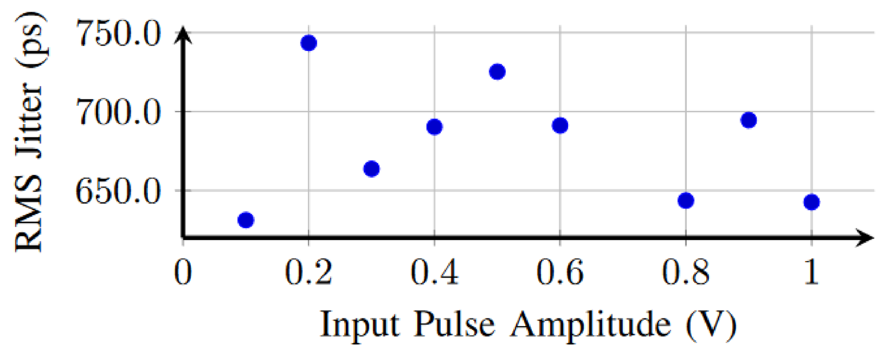
Left: One possible scenario for radiation single event effect-induced lockout. The CFD output remains low, and the system never resets the peak detector until the chip is reconfigured.
Right: The single event transient (SET) detection/correction watchdog circuit and operation in the event of an otherwise lock-inducing transient.
(1) An SET causes the peak detector output to trigger the LED, starting the LED one-shot timer.
(2) If the CFD has not registered an event after t_{stuck}, rst_stuck raises,
(3) resetting the peak detector along with the LED (and CFD) outputs.

Results



Parameter	Values
Minimum Detectable Signal	8-10Me-
Maximum Event Rate	>10Mevents/s
Timing Walk (over 10× Amplitude)	601ps
Jitter	$743ps_{rms}$
Power	$2.9mA \times 3.3V_{DD,IO}$ ($1.8V_{DD,core}$)
Area	1.6mm × 1.7mm





Conclusions

Modified constant fraction discriminator architecture:

- ✓ Maintains theoretical zero timing walk of conventional CFDs
- ✓ Trigger fraction stays at a constant f, irrespective of pulse shape
- ✓ Extended range for internal delay from pulse width to timing between pulses

Designed and tested ASIC:

- ✓ Sub-nanosecond timing walk
- ✓ Sub-nanosecond RMS jitter
- ✓ Afterpulse rejection with an output monostable multivibrator
- ✓ SEU immunity with DICE latches and triple redundant gates
- ✓ Watchdog to detect and correct SEE-induced lockout
- ✓ Average current of 3.3mA from an on-chip 1.8V regulator

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